What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A metal-polysilicon contact providing electrical connection on a substrate, said metal-polysilicon contact comprising:

a polysilicon layer;

a barrier layer formed over said polysilicon layer;

at least one conductive layer formed over said barrier layer; and

at least one oxygen sink layer formed adjacent to said conductive layer, said oxygen sink layer being capable of absorbing oxygen.

2. The metal-polysilicon contact of claim 1, wherein said conductive layer is formed in an opening of an insulating layer, said conductive layer having at least one vertically extending surface in said opening.

3. The metal-polysilicon contact of claim 2, wherein said oxygen sink layer contacts said conductive layer at said at least one vertically extended surface.

4. The metal-polysilicon contact of claim 1, wherein said conductive layer is made of a material which is conductive when oxidized.

5. The metal-polysilicon contact of claim 1, wherein said conductive layer comprises a platinum layer.

6. The metal-polysilicon contact of claim 1, wherein said conductive layer comprises a platinum oxide layer.

7. The metal-polysilicon contact of claim 1, wherein said conductive layer comprises an iridium layer.

8. The metal-polysilicon contact of claim 1, wherein said conductive layer comprises an iridium oxide layer.

9. The metal-polysilicon contact of claim 1, wherein said conductive layer comprises a ruthenium layer.

10. The metal-polysilicon contact of claim 1, wherein said conductive layer comprises a ruthenium oxide layer.

11. The metal-polysilicon contact of claim 1, wherein said conductive layer comprises a rhodium layer.

12. The metal-polysilicon contact of claim 1, wherein said conductive layer comprises a rhodium oxide layer.

13. The metal-polysilicon contact of claim 1, wherein said barrier layer is formed of a material selected from the group consisting of refractory metal nitrides, refractory metal carbides, and refractory metal borides.

14. The metal-polysilicon contact of claim 1, wherein said barrier layer is formed of $TiSi_2$.

15. The metal-polysilicon contact of claim 1, wherein said barrier layer has a thickness of approximately 60 to 200 Angstroms.

16. The metal-polysilicon contact of claim 1, wherein said conductive layer has a thickness of approximately 100 to 300 Angstroms.

17. The metal-polysilicon contact of claim 1, wherein said oxygen sink layer is formed of a material selected from the group consisting of polysilicon, aluminum nitride, titanium nitride, tantalum, and silicon nitride.

18. The metal-polysilicon contact of claim 1, wherein said oxygen sink layer is formed of titanium.

19. The metal-polysilicon contact of claim 1 further comprising a capacitor formed over and in contact with said conductive layer.

20. The metal-polysilicon contact of claim 1, wherein said metal-polysilicon contact is a high aspect ratio contact.

21. The metal-polysilicon contact of claim 20, wherein said high aspect ratio contact has an aspect ratio of at least 25.

22. The metal-polysilicon contact of claim 1, wherein said metal-polysilicon is part of a memory circuit.

23. The metal-polysilicon contact of claim 1, wherein said substrate is a semiconductor substrate.

24. The metal-polysilicon contact of claim 23, wherein said semiconductor substrate is a silicon substrate.

25. The metal-polysilicon contact of claim 23, wherein said semiconductor substrate is a germanium substrate.

26. The metal-polysilicon contact of claim 23, wherein said semiconductor substrate is a gallium arsenide substrate.

27. The metal-polysilicon contact of claim 1, wherein said at least one oxygen sink layer comprises a plurality of spaced oxygen sink layers.

28. The metal-polysilicon contact of claim 27, wherein said plurality of spaced oxygen sink layers comprises two oxygen sink layers separated by one conductive layer.

29. The metal-polysilicon contact of claim 27, wherein said plurality of oxygen sink layers comprises three spaced oxygen sink layers separated by two contacting conductive layers.

30. The metal-polysilicon contact of claim 1 further comprising at least one oxygen barrier layer provided between said oxygen sink layer and said conductive layer.

31. The metal-polysilicon contact of claim 30, wherein said oxygen barrier layer is formed of silicon nitride.

32. The metal-polysilicon contact of claim 31, wherein said oxygen sink layer is formed of titanium.

33. A method for fabricating a metal-polysilicon contact in a semiconductor device, comprising the steps of:

forming an insulating layer over a barrier layer residing over a polysilicon layer;

forming a contact opening in said insulating layer; and

forming at least one conductive layer and at least one oxygen sink layer in said contact opening, said oxygen sink layer being capable of absorbing oxygen.

34. The method of claim 33, wherein said conductive layer is formed adjacent to said oxygen sink layer.

35. The method of claim 33, wherein said conductive layer is formed of a material which is conductive when oxidized.

36. The method of claim 33, wherein said conductive layer comprises a platinum layer.

37. The method of claim 33, wherein said conductive layer comprises a platinum oxide layer.

38. The method of claim 33, wherein said conductive layer comprises an iridium layer.

39. The method of claim 33, wherein said conductive layer comprises an iridium oxide layer.

40. The method of claim 33, wherein said conductive layer comprises a ruthenium layer.

41. The method of claim 33, wherein said conductive layer comprises a ruthenium oxide layer.

42. The method of claim 33, wherein said conductive layer comprises a rhodium layer.

43. The method of claim 33, wherein said conductive layer comprises a rhodium oxide layer.

44. The method of claim 33, wherein said barrier layer is formed of a material selected from the group consisting of refractory metal nitrides, refractory metal carbides, and refractory metal borides.

45. The method of claim 33, wherein said barrier layer is formed of $TiSi_2$.

47. The method of claim 33, wherein said barrier layer has a thickness of approximately 60 to 200 Angstroms.

48. The method of claim 33, wherein said metal layer has a thickness of approximately 100 to 300 Angstroms.

49. The method of claim 33, wherein said oxygen sink layer is formed of a material selected from the group consisting of polysilicon, aluminum nitride, titanium nitride, tantalum, and silicon nitride.

50. The method of claim 33, wherein said oxygen sink layer is formed of titanium.

51. The method of claim 33, wherein said at least one oxygen sink layer is formed as a plurality of spaced oxygen sink layers.

52. The method of claim 51, wherein said plurality of spaced oxygen sink layers comprises two oxygen sink layers separated by one conductive layer.

53. The method of claim 51, wherein said plurality of spaced oxygen sink layers comprises three oxygen sink layers separated by two contacting conductive layers.

54. The method of claim 33 further comprising at least one oxygen barrier layer provided between said oxygen sink layer and said conductive layer.

55. The method of claim 54, wherein said oxygen barrier layer is formed of silicon nitride.

56. The method of claim 55, wherein said oxygen sink layer is formed of titanium.

57. The method of claim 33, wherein said step of forming said barrier layer includes sputtering.

58. The method of claim 33, wherein said step of forming said contact opening includes etching of said insulating layer.

59. The method of claim 33, wherein said step of forming said at least one oxygen sink layer includes sputtering.

60. The method of claim 33 further comprising the step of forming a semiconductor device over said metal-polysilicon contact.

61. The method of claim 60, wherein said semiconductor device is a capacitor.

62. The method of claim 60, wherein said semiconductor device is part of an integrated circuit.

63. A processor-based system, comprising:

a processor; and

a memory circuit coupled to said processor, at least one of said processor and said memory circuit containing a metal-polysilicon contact, said metal-polysilicon contact comprising a polysilicon layer formed over a substrate; a barrier layer formed over said polysilicon layer; at least one conductive layer formed over said barrier layer; and at least one oxygen sink layer formed adjacent to said conductive layer, said oxygen sink layer being capable of absorbing oxygen.

64. The processor-based system of claim 63, wherein said conductive layer is formed in an opening of an insulating layer, said conductive layer having at least one vertically extended surface in said opening.

65. The processor-based system of claim 63, wherein said oxygen sink layer contacts said conductive layer at said at least one vertically extended surface.

66. The processor-based system of claim 63, wherein said conductive layer is made of a material which is conductive when oxidized.

67. The processor-based system of claim 63, wherein said conductive layer comprises a platinum layer.

68. The processor-based system of claim 63, wherein said conductive layer comprises a platinum oxide layer.

69. The processor-based system of claim 63, wherein said conductive layer comprises an iridium layer.

70. The processor-based system of claim 63, wherein said conductive layer comprises an iridium oxide layer.

71. The processor-based system of claim 63, wherein said conductive layer comprises a ruthenium layer.

72. The processor-based system of claim 63, wherein said conductive layer comprises a ruthenium oxide layer.

73. The processor-based system of claim 63, wherein said conductive layer comprises a rhodium layer.

74. The processor-based system of claim 63, wherein said conductive layer comprises a rhodium oxide layer.

75. The processor-based system of claim 63, wherein said barrier layer is formed of a material selected from the group consisting of refractory metal nitrides, refractory metal carbides, and refractory metal borides.

76. The processor-based system of claim 63, wherein said oxygen sink layer is formed of a material selected from the group consisting of polysilicon, aluminum nitride, titanium nitride, tantalum, and silicon nitride.

77. The processor-based system of claim 63 further comprising a capacitor formed over and in contact with said conductive layer.

78. The processor-based system of claim 63, wherein said metal-polysilicon contact is a high aspect ratio contact.

79. The processor-based system of claim 63, wherein said high aspect ratio contact has an aspect ration of at least 25.

80. The processor-based system of claim 63, wherein said substrate is a semiconductor substrate.

81. The processor-based system of claim 80, wherein said semiconductor substrate is a silicon substrate.

82. The processor-based system of claim 80, wherein said semiconductor substrate is a germanium substrate.

83. The processor-based system of claim 80, wherein said semiconductor substrate is a gallium arsenide substrate.

84. The processor-based system of claim 63, wherein said metal-polysilicon contact is part of said processor.

85. The processor-based system of claim 63, wherein said metal-polysilicon contact is part of said memory circuit.

86. A memory cell, comprising:

a substrate;

a transistor including a gate fabricated on said substrate and including a source/drain region in said substrate disposed adjacent to said gate;

a capacitor including an electrode, said electrode having a surface aligned over said source/drain region; and

a metal-polysilicon structure providing electrical contact between said source/drain region and said surface of said electrode, said metal-polysilicon structure comprising a polysilicon layer formed over said substrate; a barrier layer formed over said polysilicon layer; at least one conductive layer formed over said barrier layer; and at least one oxygen sink layer formed adjacent to said conductive layer, said oxygen sink layer being capable of absorbing oxygen.

87. The memory cell of claim 86, wherein said conductive layer is formed in an opening of an insulating layer, said conductive layer having at least one vertically extended surface in said opening.

88. The memory cell of claim 86, wherein said oxygen sink layer contacts said conductive layer at said at least one vertically extended surface.

89. The memory cell of claim 86, wherein said conductive layer is made of a material which is conductive when oxidized.

90. The memory cell of claim 86, wherein said conductive layer comprises a platinum layer.

91. The memory cell of claim 86, wherein said conductive layer comprises a platinum oxide layer.

92. The memory cell of claim 86, wherein said conductive layer comprises an iridium layer.

93. The memory cell of claim 86, wherein said conductive layer comprises an iridium oxide layer.

94. The memory cell of claim 86, wherein said conductive layer comprises a ruthenium layer.

95. The memory cell of claim 86, wherein said conductive layer comprises a ruthenium oxide layer.

96. The memory cell of claim 86, wherein said conductive layer comprises a rhodium layer.

97. The memory cell of claim 86, wherein said conductive layer comprises a rhodium oxide layer.

98. The memory cell of claim 86, wherein said barrier layer is formed of a material selected from the group consisting of refractory metal nitrides, refractory metal carbides, and refractory metal borides.

99. The memory cell of claim 86, wherein said oxygen sink layer is formed of a material selected from the group consisting of polysilicon, aluminum nitride, titanium nitride, tantalum, and silicon nitride.

100. The memory cell of claim 86, wherein said oxygen sink layer is formed of titanium.

101. The memory cell of claim 86 further comprising a capacitor formed over and in contact with said conductive layer.

102. The memory cell of claim 86, wherein said metal-polysilicon contact is a high aspect ratio contact.

103. The memory cell of claim 86, wherein said high aspect ratio contact has an aspect ratio of at least 25.

104. The memory cell of claim 86, wherein said substrate is a semiconductor substrate.

105. The memory cell of claim 86, wherein said semiconductor substrate is a silicon substrate.

106. The memory cell of claim 86, wherein said semiconductor substrate is a germanium substrate.

107. The memory cell of claim 86, wherein said semiconductor substrate is a gallium arsenide substrate.

108. The memory cell of claim 86, wherein said at least one oxygen sink layer comprises a plurality of spaced oxygen sink layers.

109. The memory cell of claim 108, wherein said plurality of spaced oxygen sink layers comprises two oxygen sink layers separated by one conductive layer.

110. The memory cell of claim 108, wherein said plurality of spaced oxygen sink layers comprises three oxygen sink layers separated by two contacting conductive layers.